Y-A133 核心板产品规格书

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修改记录

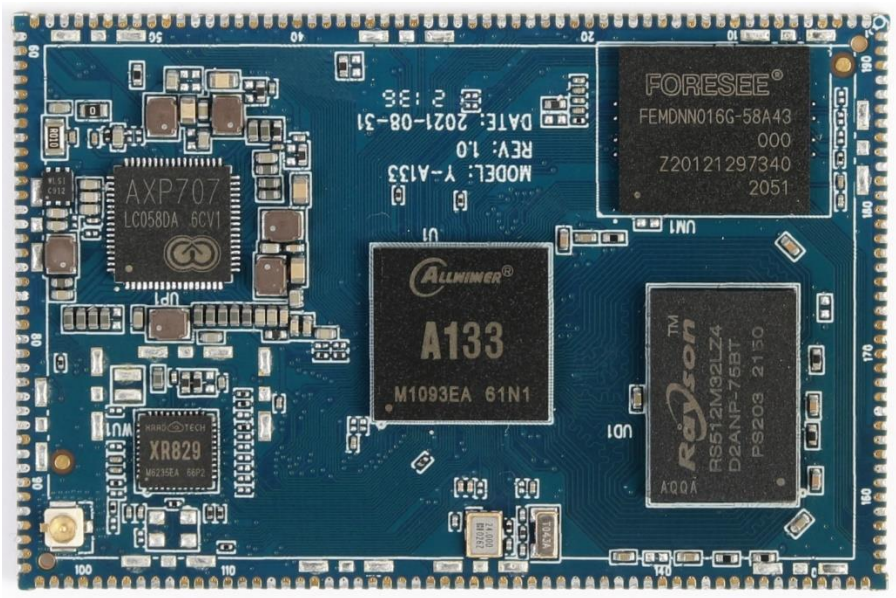
1.0.0	2023-02-06	根据 V1.0 硬件版本更新。

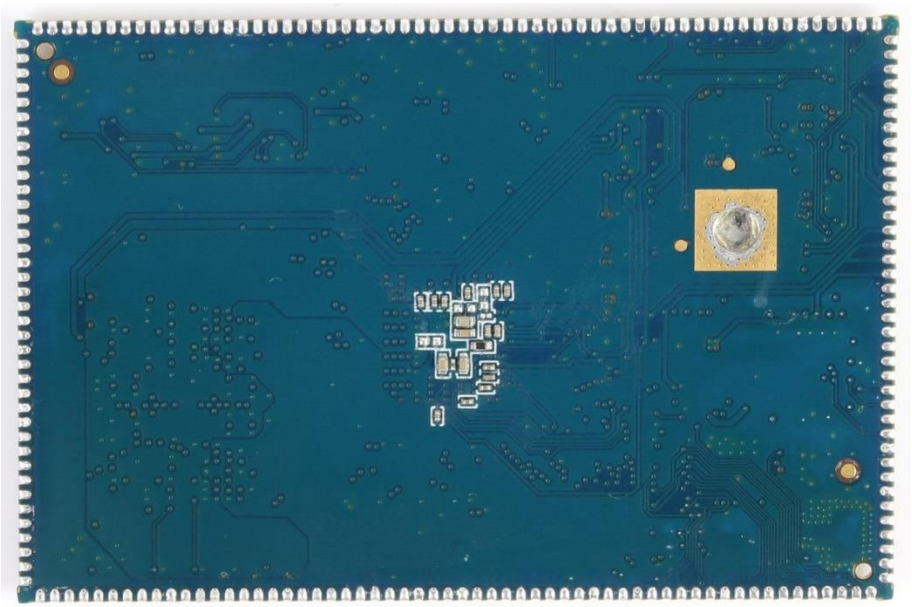
目 录

1 产品简介

Y-A133 核心板，采用 192P 接口设计，板载基于四核 64 位 Cortex-A53 处理器的 A133 主控，主频 1.6 GHz，具备超强的计算性能、2D/3D 图形处理能力和全高清视频编解码能力，完美支持 4Kx2K@60fps 超清解码和 4Kx2K HDMI 超清输出。可应用于跑步机、触摸互动、消费电子、娱乐系统等行业，提供配套的源代码、教程、技术资料和开发工具，让开发变得更加简单方便，提供多种存储配置选择，用户仅需扩展功能底板，即可快速实现项目研产。

Y-A133 核心板实物接口示意图如下所示。





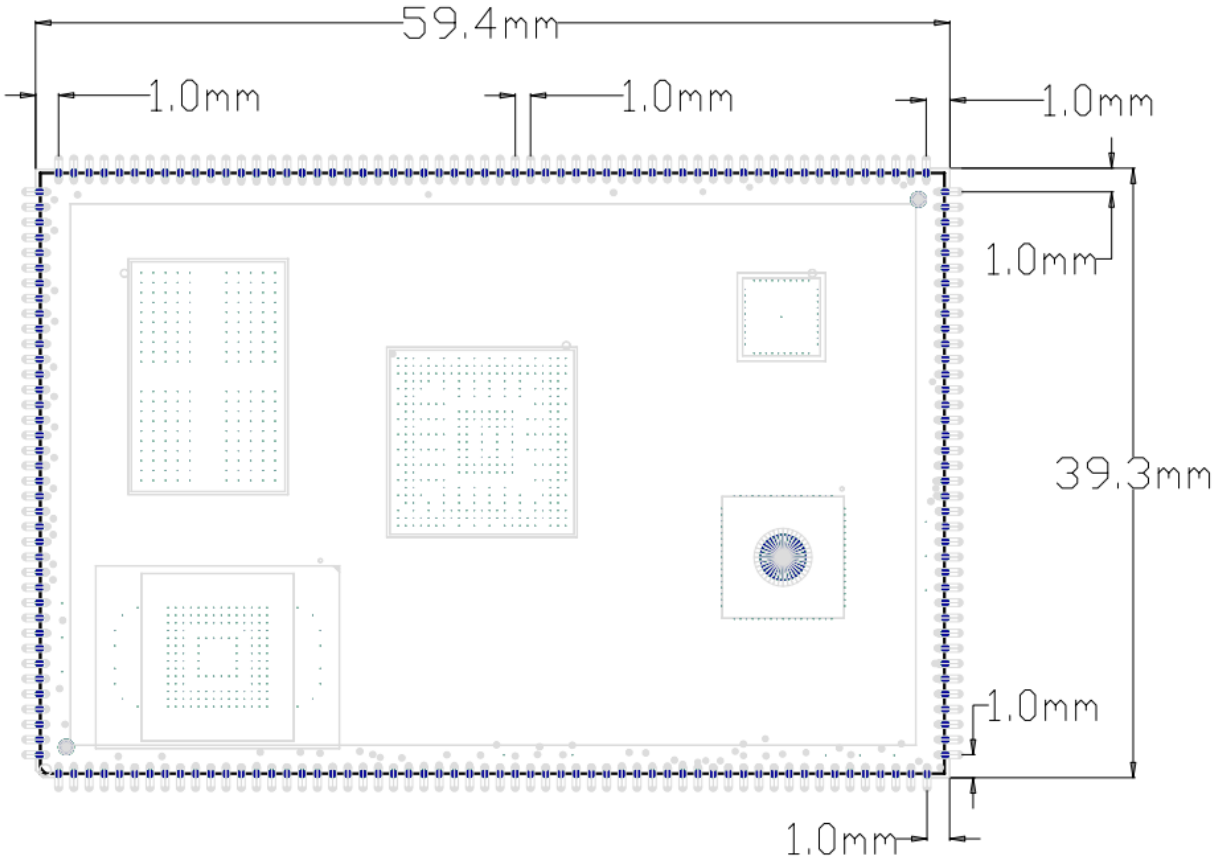
2 规格参数

Y-A133 的系统功能和接口特性如下表所示。

主要参数	
CPU	A133 四核 64 位 Cortex-A53 处理器，主频最高 1.6GHz；支持 OpenGL ES 1.1/2.0/3.2, Vulkan 1.1, OpenCL 1.2
内 存	LPDDR4 1GB（2GB|4GB 可选）
存 储	默认标配 8GB EMMC NAND 芯片，可扩展至最大 128GB
视 频	支持 4K@30fps H.265/H.264 视频解码；支持 720P@30fps VP9 视频解码 支持 1080P 100fps H.264 视频编码；支持 4K@15fps MJPEG/JPEG 基线编码
音 频	1 个 LINE-OUT、1 个 MIC-IN、1 个立体声耳机、1 个 I2S
WiFi/蓝牙	板载高性能 SDIO 3.0 接口 XR829 模块，支持 IEEE 802.11 b/g/n/ac+ BT4.2
显 示	支持 LVDS 1080P@60Hz，MIPI 1920x1200@60Hz，RGB 1024x768
USB 接口	1 个 USB2.0、1 个 USB2.0（OTG）
串 口	4 个 UART 控制器（UART0,UART1,UART2,UART3），其中 UART0 可配置为调试串口
SD/MMC	SD/MMC 3.0 接口，可扩展 SD 卡
SPI	3 个 SPI 控制器（SPI0,SPI1,SPI2）
TWI	4 个 TWI 控制器（TWI0,TWI1,TWI2, S_ TWI1），可扩展 I2C 芯片和外设
摄像头	支持 200 万像素以内 USB 摄像头；支持最高 1000 万像素的 MIPI 摄像头
以太网	1 个 10/100M 自适应以太网
电源输入	支持 5V 直流电源输入（电源误差±5%）
环境要求	工作温度-40°~85°，存储温度-40°~70°
系统支持	支持 Android 10.0、Linux 等操作系统
SDK 开发	提供完整的软件开发 SDK、开发文档、技术资料、开发教程等配套资料
核心板尺寸	59.4mm × 39.3 mm
接口类型	邮票孔（192Pin，1.0mm 间距）
PCB 规格	6 层板设计

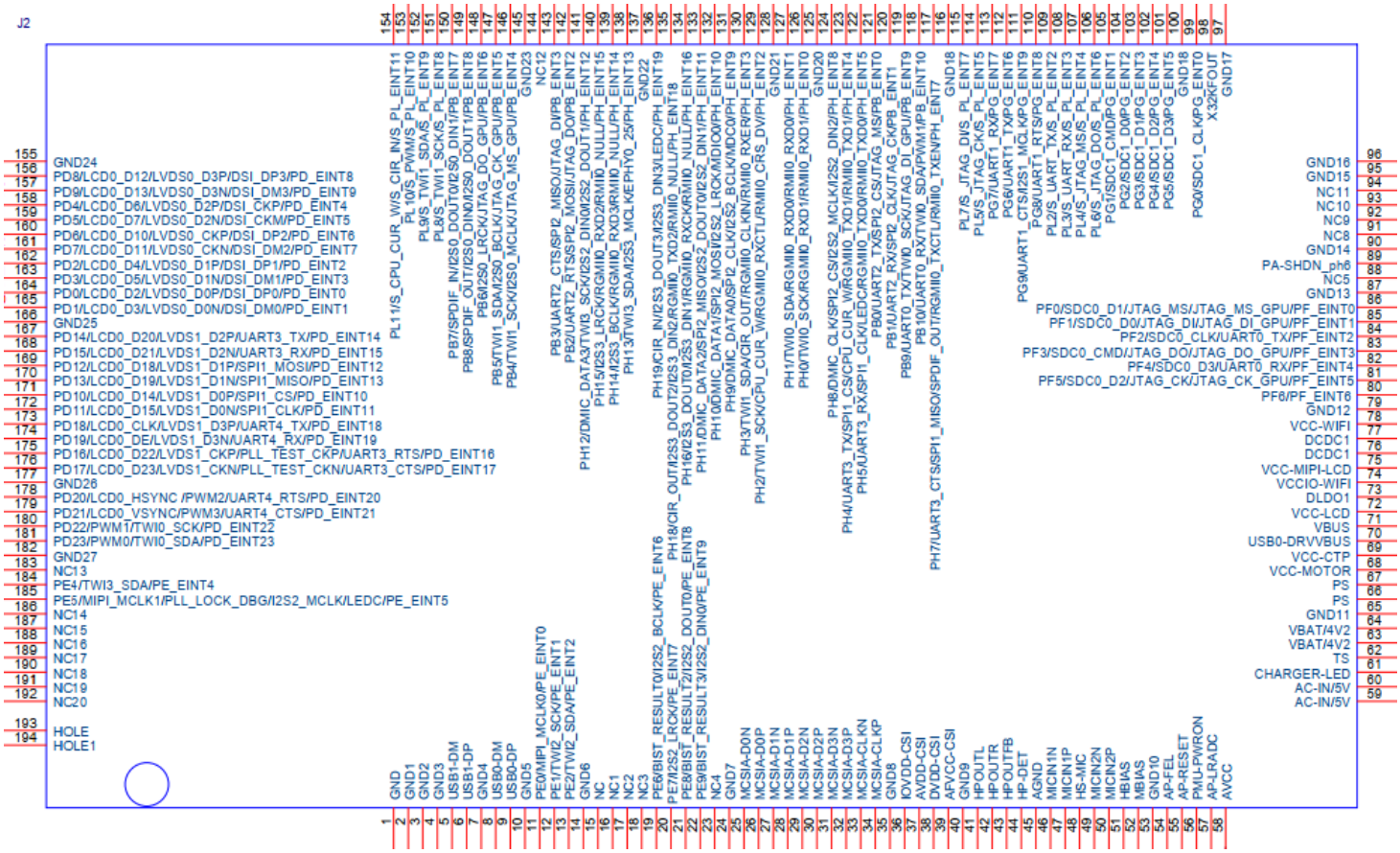
3 核心板尺寸

PCB 大小为 59.4mm*39.3mm，相应的物理尺寸参数如下图所示。



4 接口定义

Y-A133 核心板接口信号定义如下，提供了 CPU 全部的功能信号。如需自定义底板设计，详细设计阶段我司将提供参考原理图和信号说明文档。



核心板接口定义说明

Types: I = Input, O = Output, I/O = Input/Output, A = Analog, AI= Analog Input, G= Ground, P = power, AO=Analog Output, A I/O = Analog Input/Output, OD= Open-Drain, NA=Unknown

Pin	Core board pin definition	Type	IO power domain	Function for Mainboard	Default function description
1	GND	G	GND	GND	Digital Ground
2	GND1	G			
3	GND2	G			
4	GND3	G			
5	USB1-DM	A I/O	3.3V	USB1-DM	USB2.0 HOST data signal DM
6	USB1-DP	A I/O	3.3V	USB1-DP	USB2.0 HOST data signal DP
7	GND4	G	GND	GND	Digital Ground

8	USB0-DM	A I/O	3.3V	USB0-DM	USB2.0 OTG data signal DM
9	USB0-DP	A I/O	3.3V	USB0-DP	USB2.0 OTG data signal DP
10	GND5	G	GND	GND	Digital Ground
11	PE0/MIPI_MCLK0/PE_EINT0	I/O	1.8V/3.3V	MCSI-MCLK_pe0	PE0/MIPI_MCLK0/PE_EINT0
12	PE1/TWI2_SCK/PE_EINT1	I/O	1.8V/3.3V	MCSI-SCK_pe1	PE1/TWI2_SCK/PE_EINT1
13	PE2/TWI2_SDA/PE_EINT2	I/O	1.8V/3.3V	MCSI-SDA_pe2	PE2/TWI2_SDA/PE_EINT2
14	GND6	G	GND	GND	Digital Ground
15	NC	NC		NC	Not Connected
16	NC1	NC			
17	NC2	NC			
18	NC3	NC			
19	PE6/BIST_RESULT0/I2S2_BCLK/PE_EINT6	I/O	1.8V/3.3V	MCSI-STB-F_pe6	PE6/BIST_RESULT0/I2S2_BCLK/PE_EINT6
20	PE7/I2S2_LRCK/PE_EINT7	I/O	1.8V/3.3V	MCSI-RST-F_pe7	PE7/I2S2_LRCK/PE_EINT7
21	PE8/BIST_RESULT2/I2S2_DOUT0/PE_EINT8	I/O	1.8V/3.3V	MCSI-STB-R_pe8	PE8/BIST_RESULT2/I2S2_DOUT0/PE_EINT8
22	PE9/BIST_RESULT3/I2S2_DIN0/PE_EINT9	I/O	1.8V/3.3V	MCSI-RST-R_pe9	PE9/BIST_RESULT3/I2S2_DIN0/PE_EINT9
23	NC4	NC		NC	Not Connected
24	GND7	G	GND	GND	Digital Ground
25	MCSIA-D0N	AI	1.8V	MCSIA-D0N	MIPI CSI controller A data0 negative signal
26	MCSIA-D0P	AI	1.8V	MCSIA-D0P	MIPI CSI controller A data0 positive signal
27	MCSIA-D1N	AI	1.8V	MCSIA-D1N	MIPI CSI controller A data1 negative signal
28	MCSIA-D1P	AI	1.8V	MCSIA-D1P	MIPI CSI controller A data1 positive signal
29	MCSIA-D2N	AI	1.8V	MCSIA-D2N	MIPI CSI controller A data2 negative signal
30	MCSIA-D2P	AI	1.8V	MCSIA-D2P	MIPI CSI controller A data2 positive signal
31	MCSIA-D3N	AI	1.8V	MCSIA-D3N	MIPI CSI controller A data3 negative signal
32	MCSIA-D3P	AI	1.8V	MCSIA-D3P	MIPI CSI controller A data3 positive signal
33	MCSIA-CLKN	AI	1.8V	MCSIA-CLKN	MIPI CSI controller A clock negative signal
34	MCSIA-CLKP	AI	1.8V	MCSIA-CLKP	MIPI CSI controller A clock positive signal
35	GND8	G	GND	GND	Digital Ground
36	IOVDD-CSI	O	1.8V	IOVDD-CSI	Power supply for analog part CSI
37	AVDD-CSI	O	2.8V	AVDD-CSI	Power supply for analog part CSI

38	DVDD-CSI	O	2.5V	DVDD-CSI	Power supply for analog part CSI
39	AFVDD-CSI	O	2.8V	AFVDD-CSI	Power supply for analog part CSI
40	GND9	G	GND	GND	Digital Ground
41	HPOUTL	AO	1.8V	HPOUTL	Headphone left output
42	HPOUTR	AO	1.8V	HPOUTR	Headphone right output
43	HPOUTFB	AI	1.8V	HPOUTFB	Pseudo differential headphone ground reference
44	HP-DET	AI	1.8V	HP-DET	Headphone Jack detect
45	AGND	G	GND	AGND	Analog ground
46	MICIN1N	AI	1.8V	MICIN1N	Negative differential input for MIC1
47	MICIN1P	AI	1.8V	MICIN1P	Positive differential input for MIC1
48	HS-MIC	AI	3.3V	MIC_DET	HS-MIC
49	MICIN2N	AI	1.8V	MICIN2N	Negative differential input for MIC2
50	MICIN2P	AI	1.8V	MICIN2P	Positive differential input for MIC2
51	HBIAS	AO	3.3V	HBIAS	Second bias voltage output for headset microphone
52	MBIAS	AO	3.3V	MBIAS	First bias voltage output for main microphone
53	GND10	G	GND	GND	Digital Ground
54	AP-FEL	I	3.3V	AP-FEL	Boot select
55	AP-RESET	I/O	1.8V	AP-RESET	Reset signal(low active)
56	PMU-PWRON	O	1.8V	PMU-PWRON	PMU-PWRON
57	AP-LRADC	AI	1.8V	AP-LRADC	Low rate ADC input channel
58	AVCC	P	3.3V	AVCC	Power supply for analog part

Pin	Core board pin definition	Type	IO power domain	Function for Mainboard	Default function description
59	AC-IN/5V	I	5V	AC-IN	5V supply input for system
60	AC-IN/5V	I	5V	AC-IN	
61	CHARGER-LED	O	5V	CHGLED	Charger status indication
62	TS	O	3.3V	TS	Battery Temperature Sensor Input or an External ADCInput
63	VBAT/4V2	I	4.2V	VBAT	Two-cell battery supply input
64	VBAT/4V2	I	4.2V	VBAT	
65	GND11	G	GND	GND	Digital Ground
66	PS	O	5V	PS	PMU internal power output
67	PS	O	5v	PS	
68	VCC-MOTOR	O	3.3V	VCC-MOTOR	GPIO1-LDO, 3.3V or 1.8V, default off
69	VCC-CTP	O	3.3V	VCC-CTP	GPIO0-LDO, 3.3V or 1.8V, default off
70	USB0-DRVVBUS	I	5V	USB0-DRVVBUS	USB0 OTG 5V input
71	VBUS	I	5V	VBUS	USB0 HOST 5V input
72	VCC-LCD	O	3.3V	VCC-LCD	LCD power supply
73	DLDO1	O	1.8V/3.3V	DLDO1	3.3V default, 1.8V option

74	VCCIO-WIFI	O	1.8V/3.3V	VCCIO-WIFI	3.3V default, 1.8V option
75	VCC-MIPI-LCD	O	1.8V	VCC-MIPI-LCD	MIPI CSI power supply
76	DCDC1	O	3.3V	DCDC1	3.3V default, 1.8V option
77	DCDC1	O	3.3V	DCDC1	
78	VCC-WIFI	O	3.3V	VCC-WIFI	3.3V default. If DLDO1/VCCIO-WIFI is 1.8V level, RP45 should be
79	GND12	G	GND	GND	Digital Ground
80	PF6/PF_EINT6	I/O	1.8V/3.3V	SDC0-DET_pf6	
81	PF5/SDC0_D2/JTAG_CK/JTAG_CK_GPU/PF_EINT5	I/O	1.8V/3.3V	SDC0_D2	SDC0 data bit
82	PF4/SDC0_D3/UART0_RX/PF_EINT4	I/O	1.8V/3.3V	SDC0_D3	SDC0 data bit
83	PF3/SDC0_CMD/JTAG_DO/JTAG_DO_GPU/PF_EINT3	I/O	1.8V/3.3V	SDC0_CMD	SDC0 command signal
84	PF2/SDC0_CLK/UART0_TX/PF_EINT2	I/O	1.8V/3.3V	SDC0_CLK	SDC0 clock
85	PF1/SDC0_D0/JTAG_DI/JTAG_DI_GPU/PF_EINT1	I/O	1.8V/3.3V	SDC0_D0	SDC0 data bit
86	PF0/SDC0_D1/JTAG_MS/JTAG_MS_GPU/PF_EINT0	I/O	1.8V/3.3V	SDC0_D1	SDC0 data bit
87	GND13	G	GND	GND	Digital Ground
88	NC5	NC		NC	Not Connected
89	PA-SHDN_ph6	I/O	3.3V	PA-SHDN_ph6	PA-SHDN_ph6
90	GND14	G	GND	GND	Digital Ground
91	NC8	NC		NC	Not Connected
92	NC9	NC			
93	NC10	NC			
94	NC11	NC			
95	GND15	G	GND	GND	Digital Ground
96	GND16	G	GND	GND	Digital Ground

Pin	Core board pin definition	Type	IO power domain	Function for Mainboard	Default function description
97	GND17	G	GND	GND	Digital Ground
98	X32KFOUT	OD	NA	AP-CK32K-OUT	32.768 kHz clock fanout. Provides low frequency clock for external devices
99	PG0/SDC1_CLK/PG_EINT0	I/O	1.8V/3.3V	WL-SDIO-CLK	WiFi interface
100	GND18	G	GND	GND	Digital Ground
101	PG5/SDC1_D3/PG_EINT5	I/O	1.8V/3.3V	WL-SDIO-D3	WiFi interface(5G 1.8V;2.4G 3.3V)
102	PG4/SDC1_D2/PG_EINT4	I/O	1.8V/3.3V	WL-SDIO-D2	
103	PG3/SDC1_D1/PG_EINT3	I/O	1.8V/3.3V	WL-SDIO-D1	
104	PG2/SDC1_D0/PG_EINT2	I/O	1.8V/3.3V	WL-SDIO-D0	
105	PG1/SDC1_CMD/PG_EINT1	I/O	1.8V/3.3V	WL-SDIO-CMD	

106	PL6/S_JTAG_DO/S_PL_EINT6	I/O	1.8V/3.3V	WL-WAKE-AP_pl6	
107	PL4/S_JTAG_MS/S_PL_EINT4	I/O	1.8V/3.3V	AP-WAKE-BT_pl4	Bluetooth interface
108	PL3/S_UART_RX/S_PL_EINT3	I/O	1.8V/3.3V	BT-WAKE-AP_pl3	
109	PL2/S_UART_TX/S_PL_EINT2	I/O	1.8V/3.3V	BT-RESETN_pl2	
110	PG8/UART1_RTS/PG_EINT8	I/O	1.8V/3.3V	BT-UART1-CTS	
111	PG9/UART1_CTS/I2S1_MCLK/PG_EINT9	I/O	1.8V/3.3V	BT-UART1-RTS	
112	PG6/UART1_TX/PG_EINT6	I/O	1.8V/3.3V	BT-UART1-RX	
113	PG7/UART1_RX/PG_EINT7	I/O	1.8V/3.3V	BT-UART1-TX	
114	PL5/S_JTAG_CK/S_PL_EINT5	I/O	1.8V/3.3V	WL-PMU-EN_pl5	WiFi interface
115	PL7/S_JTAG_DI/S_PL_EINT7	I/O	1.8V/3.3V	PL7_3v3/1v8	PL7/S_JTAG_DI/S_PL_EINT7
116	GND18	G	GND	GND	Digital Ground
117	PH7/UART3_CTS/SPI1_MISO/SPDIF_OUT/RGMII0_TXCTL/RMII0_TXEN/PH_EINT7	I/O	3.3V	PA-PWRON_ph7	PH7/UART3_CTS/SPI1_MISO/SPDIF_OUT/RGMII0_TXCTL/RMII0_TXEN/PH_EINT7
118	PB10/UART0_RX/TWI0_SDA/PWM1/PB_EINT10	I/O	3.3V	UART0_RX_pb10	UART0 data receive
119	PB9/UART0_TX/TWI0_SCK/JTAG_DI_GPU/PB_EINT9	I/O	3.3V	UART0_TX_pb9	UART0 data transmit
120	PB1/UART2_RX/SPI2_CLK/JTAG_CK/PB_EINT1	I/O	3.3V	UART2_RX_pb1	UART2 data receive
121	PB0/UART2_TX/SPI2_CS/JTAG_MS/PB_EINT0	I/O	3.3V	UART2_TX_pb0	UART2 data transmit
122	PH5/UART3_RX/SPI1_CLK/LEDC/RGMII0_TXD0/RMII0_TXD0/PH_EINT5	I/O	3.3V	UART3_RX_Ph5	UART3 data receive
123	PH4/UART3_TX/SPI1_CS/CPU_CUR_W/RGMII0_TXD1/RMII0_TXD1/PH_EINT4	I/O	3.3V	UART3_TX_Ph4	UART3 data transmit
124	PH8/DMIC_CLK/SPI2_CS/I2S2_MCLK/I2S2_DIN2/PH_EINT8	I/O	3.3V	PH8/SPI2_CS	SPI2 chip select signal, low active
125	GND20	G	GND	GND	Digital Ground
126	PH0/TWI0_SCK/RGMII0_RXD1/RMII0_RXD1/PH_EINT0	I/O	3.3V	TWI0-Sck_ph0	TWI0 serial clock signal
127	PH1/TWI0_SDA/RGMII0_RXD0/RMII0_RXD0/PH_EINT1	I/O	3.3V	TWI0-SDA_ph1	TWI0 serial data signal
128	GND21	G	GND	GND	Digital Ground
129	PH2/TWI1_SCK/CPU_CUR_W/RGMII0_RXCTL/RMII0_CRS_DV/PH_EINT2	I/O	3.3V	SENSOR-Sck_ph2	TWI1 serial clock signal
130	PH3/TWI1_SDA/CIR_OUT/RGMII0_CLKIN/RMII0_RXER/PH_EINT3	I/O	3.3V	SENSOR-SDA_ph3	TWI1 serial data signal

131	PH9/DMIC_DATA0/SPI2_CLK/I2S2_BCLK/MDC0/PH_EINT9	I/O	3.3V	PH9/SPI2_CLK	SPI2 clock signal
132	PH10/DMIC_DATA1/SPI2_MOSI/2S2_LRCK/MDIO0/PH_EINT10	I/O	3.3V	PH10/SPI2_MOSI	SPI1 master data out, slave data in
133	PH11/DMIC_DATA2/SPI2_MISO/I2S2_DOUT0/I2S2_DIN1/PH_EINT11	I/O	3.3V	PH11/SPI2_MISO	SPI1 master data in, slave data out
134	PH16/I2S3_DOUT0/I2S3_DIN1/RGMII0_RXCK/RMII0_NULL/PH_EINT16	I/O	3.3V	SYS-WORK-ON_ph16	PH16/I2S3_DOUT0/I2S3_DIN1/RGMII0_RXCK/RMII0_NULL/PH_EINT16
135	PH18/CIR_OUT/I2S3_DOUT2/I2S3_DIN2/RGMII0_TXD2/RMII0_NULL/PH_EINT18	I/O	3.3V	LCD-BL-EN_ph18	PH18/CIR_OUT/I2S3_DOUT2/I2S3_DIN2/RGMII0_TXD2/RMII0_NULL/PH_EINT18
136	PH19/CIR_IN/I2S3_DOUT3/I2S3_DIN3/LEDC/PH_EINT19	I/O	3.3V	USB0-ID-SOC_ph19	PH19/CIR_IN/I2S3_DOUT3/I2S3_DIN3/LEDC/PH_EINT19
137	GND22	G	GND	GND	Digital Ground
138	PH13/TWI3_SDA/I2S3_MCLK/EPHY0_25/PH_EINT13	I/O	3.3V	TP-INT_ph13	Interrupt input
139	PH14/I2S3_BCLK/RGMII0_RXD3/RMII0_NULL/PH_EINT14	I/O	3.3V	TP-RST_ph14	Mainboard reset output
140	PH15/I2S3_LRCK/RGMII0_RXD2/RMII0_NULL/PH_EINT15	I/O	3.3V	IR-CPU_ph15	level Irda remote control input singal
141	PH12/DMIC_DATA3/TWI3_SCK/I2S2_DIN0/I2S2_DOUT1/PH_EINT12	I/O	3.3V	LCD-PON_ph12	PH12/DMIC_DATA3/TWI3_SCK/I2S2_DIN0/I2S2_DOUT1/PH_EINT12
142	PB2/UART2_RTS/SPI2_MOSI/JTAG_DO/PB_EINT2	I/O	3.3V	4G-PON_pb2	PB2/UART2_RTS/SPI2_MOSI/JTAG_DO/PB_EINT2
143	PB3/UART2_CTS/SPI2_MISO/JTAG_DI/PB_EINT3	I/O	3.3V	4G-RST_pb3	PB3/UART2_CTS/SPI2_MISO/JTAG_DI/PB_EINT3
144	NC12	NC		NC	Not Connected
145	GND23	G	GND	GND	Digital Ground
146	PB4/TWI1_SCK/I2S0_MCLK/JTAG_MS_GPU/PB_EINT4	I/O	3.3V	PB4/I2S0-MCLK	I2S0 master clock
147	PB5/TWI1_SDA/I2S0_BCLK/JTAG_CK_GPU/PB_EINT5	I/O	3.3V	PB5/I2S0-BCLK	I2S0/PCM0 sample rate clock
148	PB6/I2S0_LRCK/JTAG_DO_GPU/PB_EINT6	I/O	3.3V	PB6/I2S0-LRCK	I2S0/PCM0 sample rate clock/sync
149	PB8/SPDIF_OUT/I2S0_DINO/I2So_DOUT1/PB_EINT8	I/O	3.3V	PB8/I2S0-DIN	I2S0/PCM0 serial data input channel
150	PB7/SPDIF_IN/I2S0_DOUTO/I2SO_DIN1/PB_EINT7	I/O	3.3V	PWR-HOLD_pb7	PB7/SPDIF_IN/I2S0_DOUTO/I2SO_DIN1/PB_EINT7
151	PL8/S_TWl1_SCK/S_PL_EINT8	I/O	5V	USB1-DRVVBUS_pl8	USB1 host 5V input

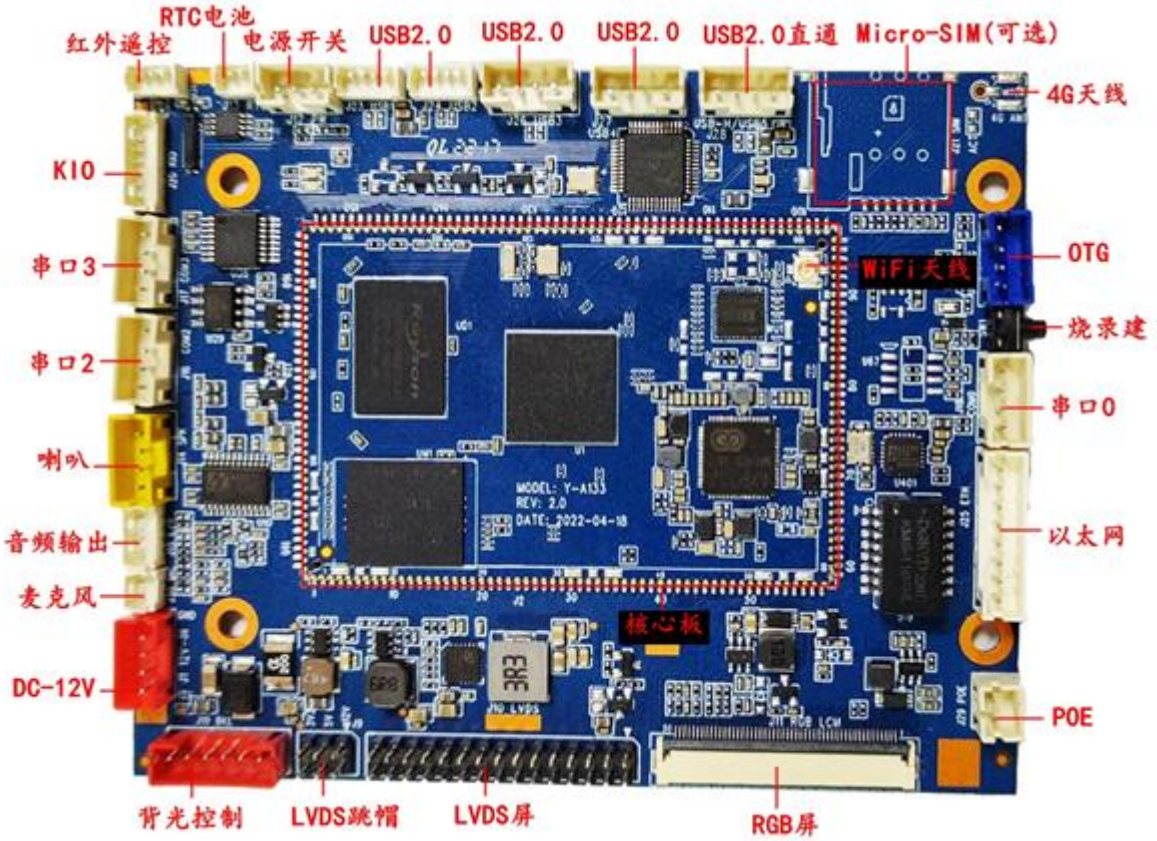
152	PL9/S_TWI1_SDA/S_PL_EINT9	I/O	1.8V/3.3V	PL9_3v3/1v8	PL9/S_TWI1_SDA/S_PL_EINT9
153	PL10/S_PWM/S_PL_EINT10	I/O	1.8V/3.3V	PL10/S_PWM_3v3/1v8	PL10/S_PWM/S_PL_EINT10
154	PL11/S_CPU_CUR_WIS_CIR_IN/S_PL_EINT11	I/O	1.8V/3.3V	PL11_3v3/1v8	PL11/S_CPU_CUR_WIS_CIR_IN/S_PL_EINT11

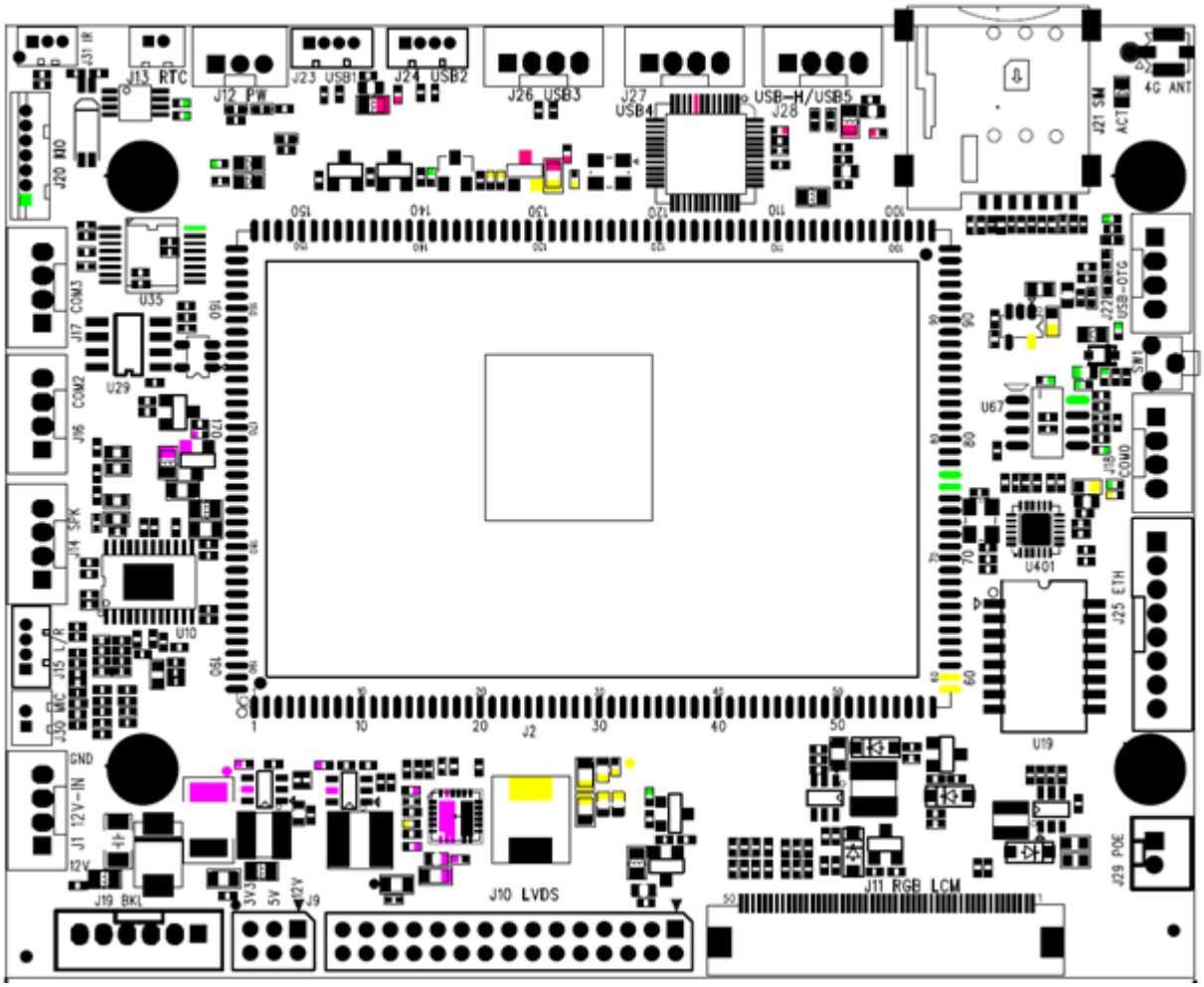
Pin	Core board pin definition	Type	IO power domain	Function for Mainboard	Default function description
155	GND24	G	GND	GND	Digital Ground
156	PD8/LCD0_D12/LVDS0_D3P/DSI_DP3/PD_EINT8	I/O	1.8V/3.3V	LCD-D12	LCD-G4/LVDS0_D3P/DSI0-DP3
157	PD9/LCD0_D13/LVDS0_D3N/DSI_DM3/PD_EINT9	I/O	1.8V/3.3V	LCD-D13	LCD-G5/LVDS0_D3N/DSI0-DM3
158	PD4/LCD0_D6/LVDS0_D2P/DSI_CKP/PD_EINT4	I/O	1.8V/3.3V	LCD-D6	LCD-B6/LVDS0_D2P/DSI0-CKP
159	PD5/LCD0_D7/LVDS0_D2N/DSI_CKM/PD_EINT5	I/O	1.8V/3.3V	LCD-D7	LCD-B7/LVDS0_D2N/DSI0-CKM
160	PD6/LCD0_D10/LVDS0_CKP/DSI_DP2/PD_EINT6	I/O	1.8V/3.3V	LCD-D10	LCD-G2/LVDS0_CKP/DSI0-DP2
161	PD7/LCD0_D11/LVDS0_CKN/DSI_DM2/PD_EINT7	I/O	1.8V/3.3V	LCD-D11	LCD-G3/LVDS0_CKN/DSI0-DM2
162	PD2/LCD0_D4/LVDS0_D1P/DSI_DP1/PD_EINT2	I/O	1.8V/3.3V	LCD-D4	LCD-B4/LVDS0_D1P/DSI0-DP1
163	PD3/LCD0_D5/LVDS0_D1N/DSI_DM1/PD_EINT3	I/O	1.8V/3.3V	LCD-D5	LCD-B5/LVDS0_D1N/DSI0-DM1
164	PDO/LCD0_D2/LVDS0_D0P/DSI_DP0/PD_EINT0	I/O	1.8V/3.3V	LCD-D2	LCD-B2/LVDS0_D0P/DSI0-DP0
165	PD1/LCD0_D3/LVDS0_D0N/DSI_DM0/PD_EINT1	I/O	1.8V/3.3V	LCD-D3	LCD-B3/LVDS0_D0N/DSI0-DM0
166	GND25	G	GND	GND	Digital Ground
167	PD14/LCD0_D20/LVDS1_D2P/UART3_TX/PD_EINT14	I/O	1.8V/3.3V	LCD-D20	LCD-R4/LVDS1_D2P
168	PD15/LCD0_D21/LVDS1_D2N/UART3_RX/PD_EINT15	I/O	1.8V/3.3V	LCD-D21	LCD-R5/LVDS1_D2N
169	PD12/LCD0_D18/LVDS1_D1P/SPI1_MOSI/PD_EINT12	I/O	1.8V/3.3V	LCD-D18	LCD-R2/LVDS1_D1P
170	PD13/LCD0_D19/LVDS1_D1N/SPI1_MISO/PD_EINT13	I/O	1.8V/3.3V	LCD-D19	LCD-R3/LVDS1_D1N
171	PD10/LCD0_D14/LVDS1_D0P/SPI1_CS/PD_EINT10	I/O	1.8V/3.3V	LCD-D14	LCD-G6/LVDS1_D0P
172	PD11/LCD0_D15/LVDS1_D0N/SPI1_CLK/PD_EINT11	I/O	1.8V/3.3V	LCD-D15	LCD-G7/LVDS1_D0N
173	PD18/LCD0_CLK/LVDS1_D3P/UART4_TX/PD_EINT18	I/O	1.8V/3.3V	LCD-CLK	LCD-CLK/LVDS1_D3P, LCD clock signal

174	PD19/LCD0_DE/LVDS1_D3N/UART4_RX/PD_EINT19	I/O	1.8V/3.3V	LCD-DE	LCD-DE/LVDS1_D3N, LCD data enable
175	PD16/LCD0_D22/LVDS1_CKP/PLL_TEST_CKP/UART3_RTS/PD_EINT16	I/O	1.8V/3.3V	LCD-D22	LCD-R6/LVDS1_CKP, LVDS1 differential clock positive signal
176	PD17/LCD0_D23/LVDS1_CKN/PLL_TEST_CKN/UART3_CTS/PD_EINT17	I/O	1.8V/3.3V	LCD-D23	LCD-R7/LVDS1_CKN, LVDS1 differential clock negative signal
177	GND26	G	GND	GND	Digital Ground
178	PD20/LCD0_HSYNC/PWM2/UART4_RTS/PD_EINT20	I/O	1.8V/3.3V	LCD-HSYNC	LCD horizontal sync
179	PD21/LCD0_VSYNC/PWM3/UART4_CTS/PD_EINT21	I/O	1.8V/3.3V	LCD-VSYNC	LCD vertical sync
180	PD22/PWM1/TWI0_SCK/PD_EINT22	I/O	1.8V/3.3V	LCD-RST_pd22	PD22/PWM1/TWI0_SCK/PD_EINT22
181	PD23/PWM0/TWI0_SDA/PD_EINT23	I/O	1.8V/3.3V	LCD-PWM_pd23	PD23/PWM0/TWI0_SDA/PD_EINT23
182	GND27	G	GND	GND	Digital Ground
183	NC13	NC		NC	Not Connected
184	PE4/TWI3_SDA/PE_EINT4	I/O	1.8V/3.3V	FEL-KEY_pe5	PE4/TWI3_SDA/PE_EINT4
185	PE5/MIPI_MCLK1/PLL_LOCK_DBG/I2S2_MCLK/LEDC/PE_EINT5	I/O	1.8V/3.3V	PW-KEY_pe5	PE5/MIPI_MCLK1/PLL_LOCK_DBG/I2S2_MCLK/LEDC/PE_EINT5
186	NC14	NC		NC	Not Connected
187	NC15	NC			
188	NC16	NC			
189	NC17	NC			
190	NC18	NC			
191	NC19	NC			
192	NC20	NC			

5 TM-YA133 参考板

下图为我司 TM-YA133 参考设计示意图，TM-YA133 底板的详细功能定义**请参考相应的硬件手册。**




J31 IR
J13 RTC
J12 PW
J23 USB1
J24 USB2
J26 USB3
J27 USB4
USB-H/USB5
J28
J21 SW
ACT
4G ANT
J20 MIC
U35
J17 COM3
U29
J6 COM2
J4 SPK
U10
J5 L/R
J30 MIC
GND
J1 12V-IN
12V
J19 BKL
3V3
5V
J9
J10 LVDS
J2
U67
J18 COM1
U401
J25 ETH
U19
J11 RGB LCM
J29 POE

6 资料列表

可提供核心板+底板的相关资料：（联系厂家技术提供）

- Y-A133 核心板原理图
- Y-A133 核心板机械图
- Y-A133 核心板 PCB 封装
- TM-YA133 底板原理图
- TM-YA133 底板机械图
- TM-YA133 底板 Gerb 文件
- TM-YA133 底板 BOM
- TM-YA133 主板产品规格书
- TM-YA133 用户使用指南
- 安卓 10 系统系统镜像包
- SDK 开发包